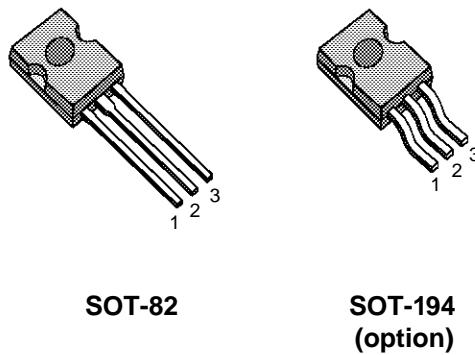


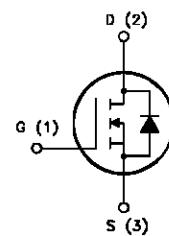
N - CHANNEL ENHANCEMENT MODE
 LOW THRESHOLD POWER MOS TRANSISTOR

TYPE	V _{DSS}	R _{DS(on)}	I _D
STK12N05L	50 V	< 0.15 Ω	12 A
STK12N06L	60 V	< 0.15 Ω	12 A

- TYPICAL R_{DS(on)} = 0.115 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- LOGIC LEVEL COMPATIBLE INPUT
- 175°C OPERATING TEMPERATURE FOR STANDARD PACKAGE
- APPLICATION ORIENTED CHARACTERIZATION


APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

INTERNAL SCHEMATIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STK12N05L	STK12N06L	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	50	60	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	50	60	V
V _{GS}	Gate-source Voltage	± 15		V
I _D	Drain Current (continuous) at T _c = 25 °C	12		A
I _D	Drain Current (continuous) at T _c = 100 °C	8		A
I _{DM(•)}	Drain Current (pulsed)	48		A
P _{tot}	Total Dissipation at T _c = 25 °C	50		W
	Derating Factor	0.33		W/°C
T _{stg}	Storage Temperature	-65 to 175		°C
T _j	Max. Operating Junction Temperature	175		°C

(•) Pulse width limited by safe operating area

STK12N05L/STK12N06L

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	3	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	80	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Case-sink	Typ	0.7	$^{\circ}\text{C}/\text{W}$
T_I	Maximum Lead Temperature For Soldering Purpose		275	$^{\circ}\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max, $\delta < 1\%$)	12	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 25\text{ V}$)	30	mJ
E_{AR}	Repetitive Avalanche Energy (pulse width limited by T_j max, $\delta < 1\%$)	7	mJ
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive ($T_c = 100^{\circ}\text{C}$, pulse width limited by T_j max, $\delta < 1\%$)	8	A

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$ for STK12N05L for STK12N06L	50 60			V V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125^{\circ}\text{C}$			250 1000	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 15\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	1	1.6	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 5\text{ V}$ $I_D = 6\text{ A}$ $V_{GS} = 5\text{ V}$ $I_D = 6\text{ A}$ $T_c = 100^{\circ}\text{C}$		0.115	0.15 0.3	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	15			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 6\text{ A}$	4	8		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		350 150 50	500 200 80	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	$V_{DD} = 25 \text{ V}$ $I_D = 6 \text{ A}$ $R_G = 50 \Omega$ $V_{GS} = 5 \text{ V}$ (see test circuit, figure 3)		55 180	80 260	ns ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 40 \text{ V}$ $I_D = 12 \text{ A}$ $R_G = 50 \Omega$ $V_{GS} = 5 \text{ V}$ (see test circuit, figure 5)		120		$\text{A}/\mu\text{s}$
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 40 \text{ V}$ $I_D = 12 \text{ A}$ $V_{GS} = 5 \text{ V}$		12 6 4	18	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 40 \text{ V}$ $I_D = 12 \text{ A}$ $R_G = 50 \Omega$ $V_{GS} = 5 \text{ V}$ (see test circuit, figure 5)		40 60 110	60 90 160	ns ns ns

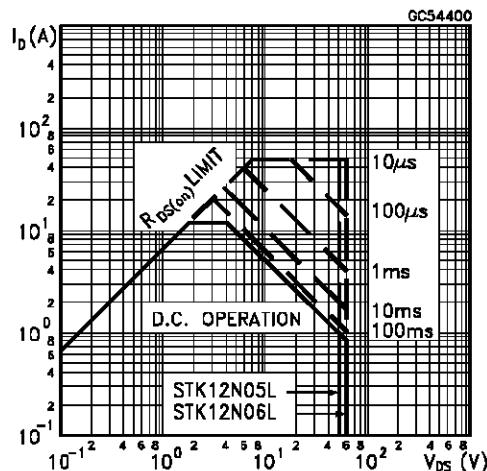
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM(\bullet)}$	Source-drain Current Source-drain Current (pulsed)				12 48	A A
$V_{SD} (\ast)$	Forward On Voltage	$I_{SD} = 12 \text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 12 \text{ A}$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 25 \text{ V}$ $T_j = 150 \text{ }^\circ\text{C}$ (see test circuit, figure 5)		75 0.15 4		ns μC A

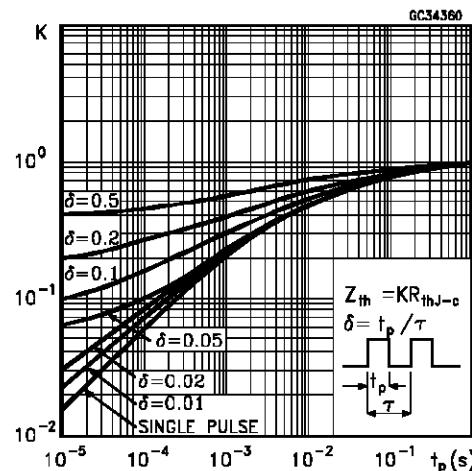
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(*) Pulse width limited by safe operating area

Safe Operating Areas

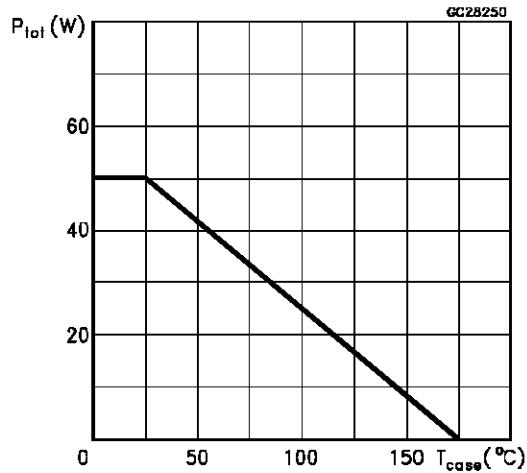


Thermal Impedance

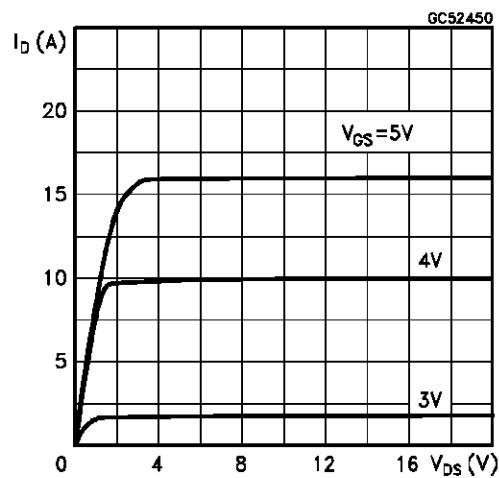


STK12N05L/STK12N06L

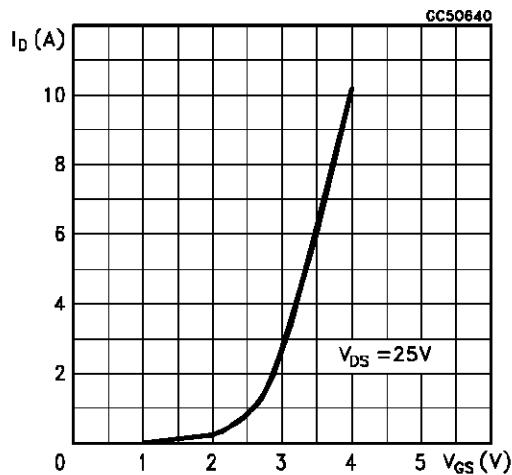
Derating Curve



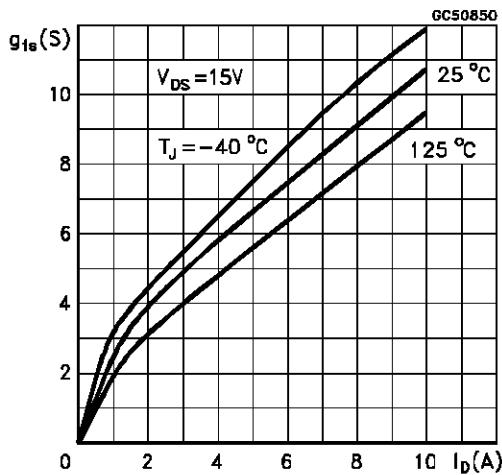
Output Characteristics



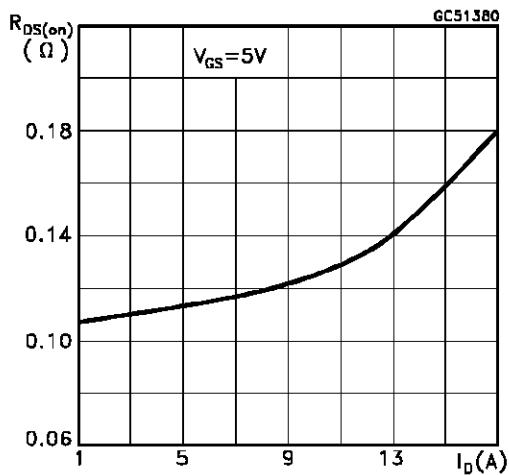
Transfer Characteristics



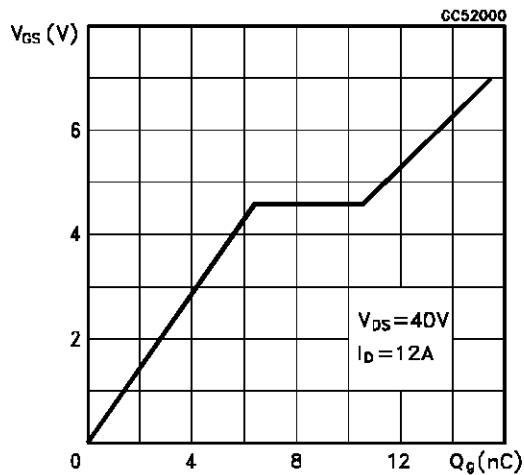
Transconductance



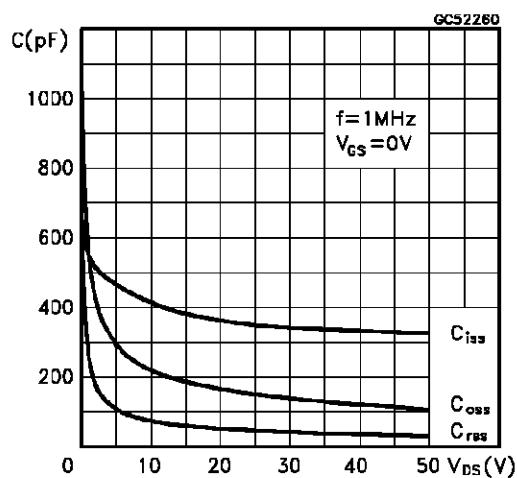
Static Drain-source On Resistance



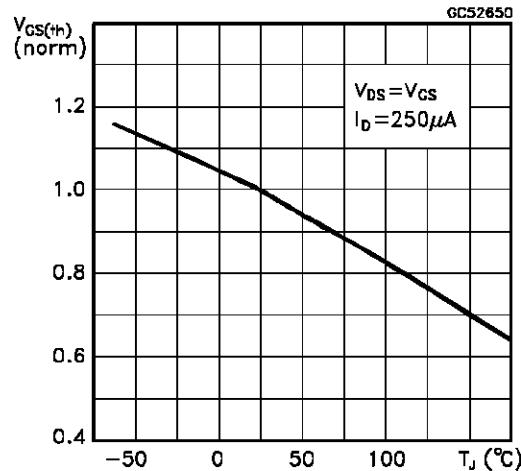
Gate Charge vs Gate-source Voltage



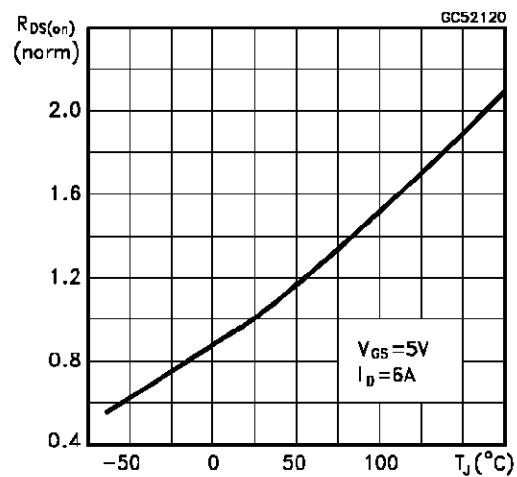
Capacitance Variations



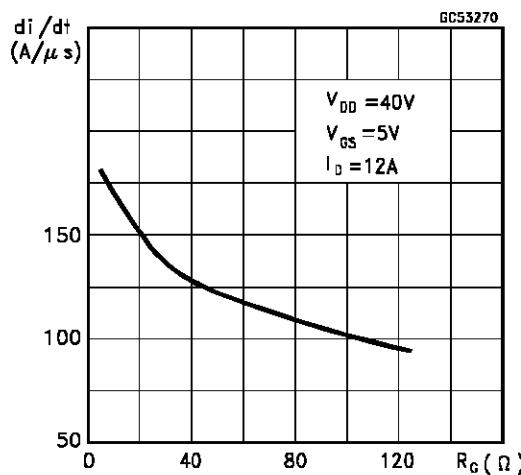
Normalized Gate Threshold Voltage vs Temperature



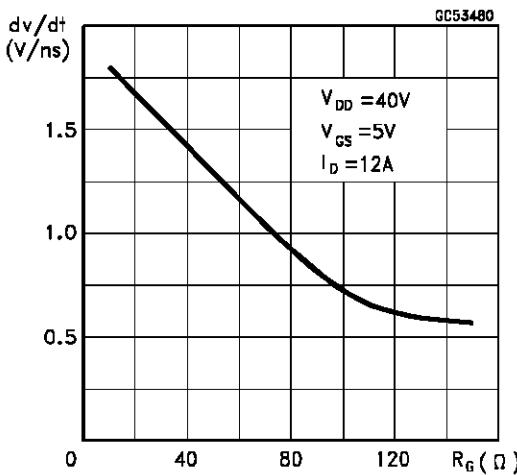
Normalized On Resistance vs Temperature



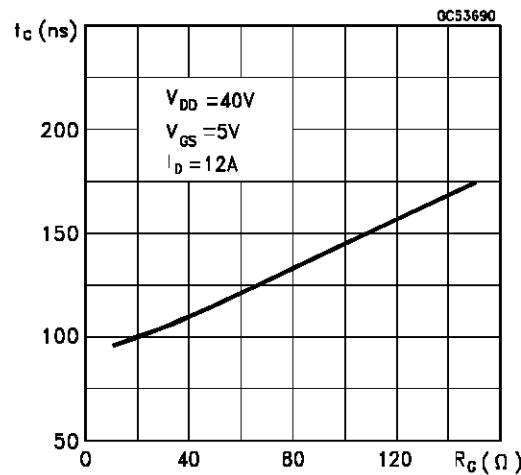
Turn-on Current Slope



Turn-off Drain-source Voltage Slope

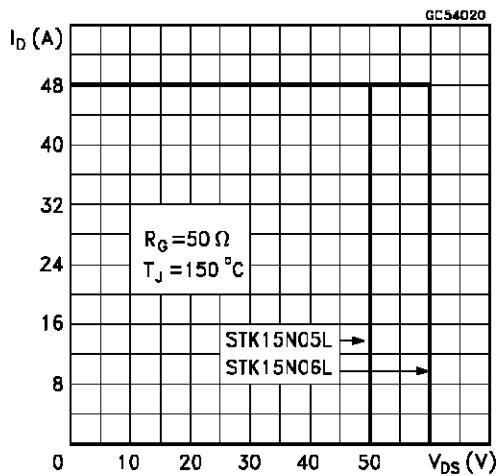


Cross-over Time

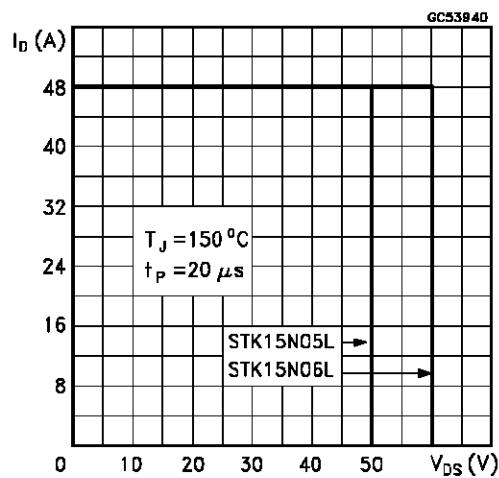


STK12N05L/STK12N06L

Switching Safe Operating Area



Accidental Overload Area



Source-drain Diode Forward Characteristics

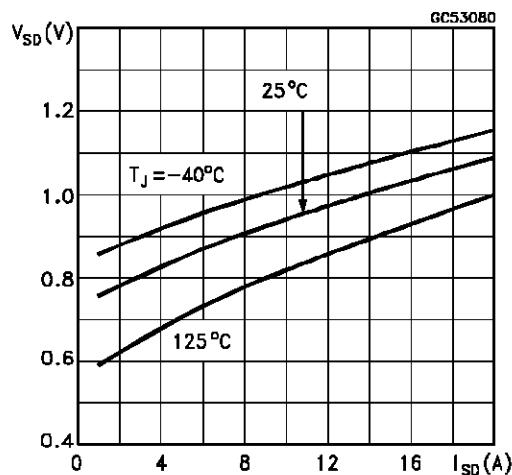


Fig. 1: Unclamped Inductive Load Test Circuits

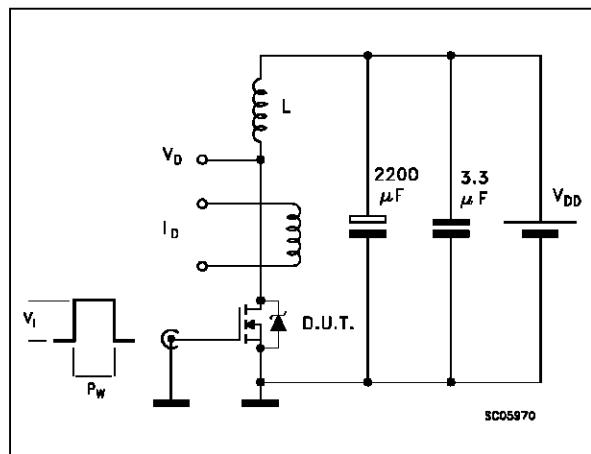


Fig. 2: Unclamped Inductive Waveforms

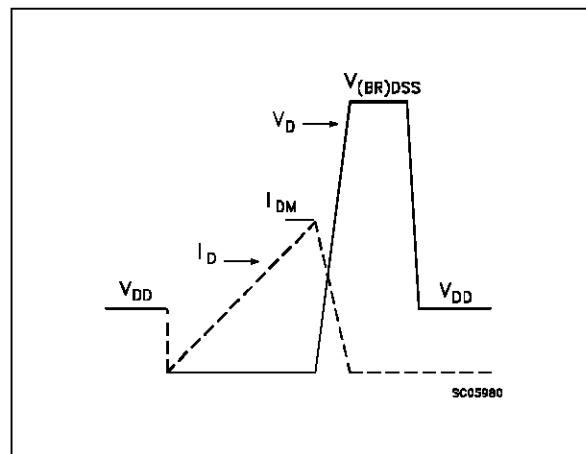


Fig. 3: Switching Times Test Circuits For Resistive Load

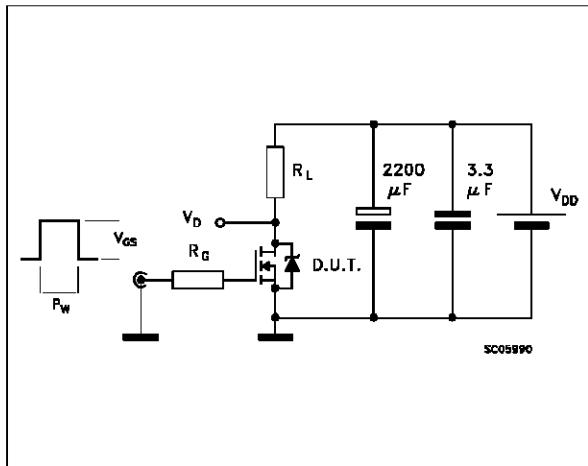


Fig. 4: Gate Charge Test Circuit

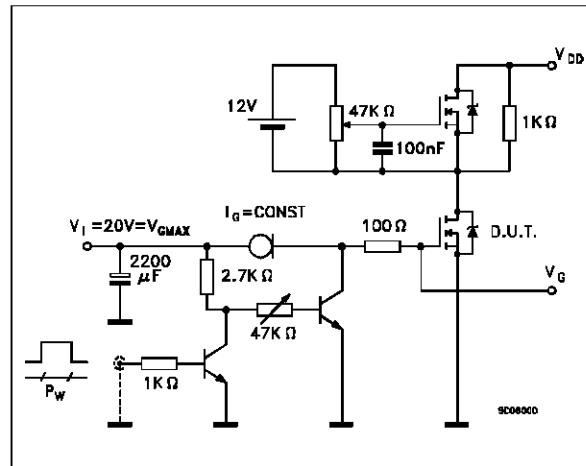
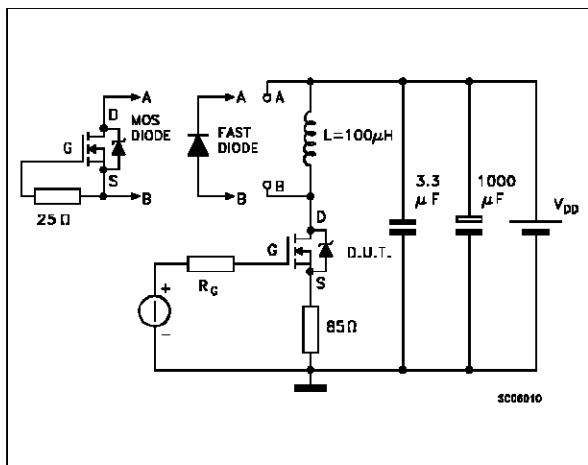
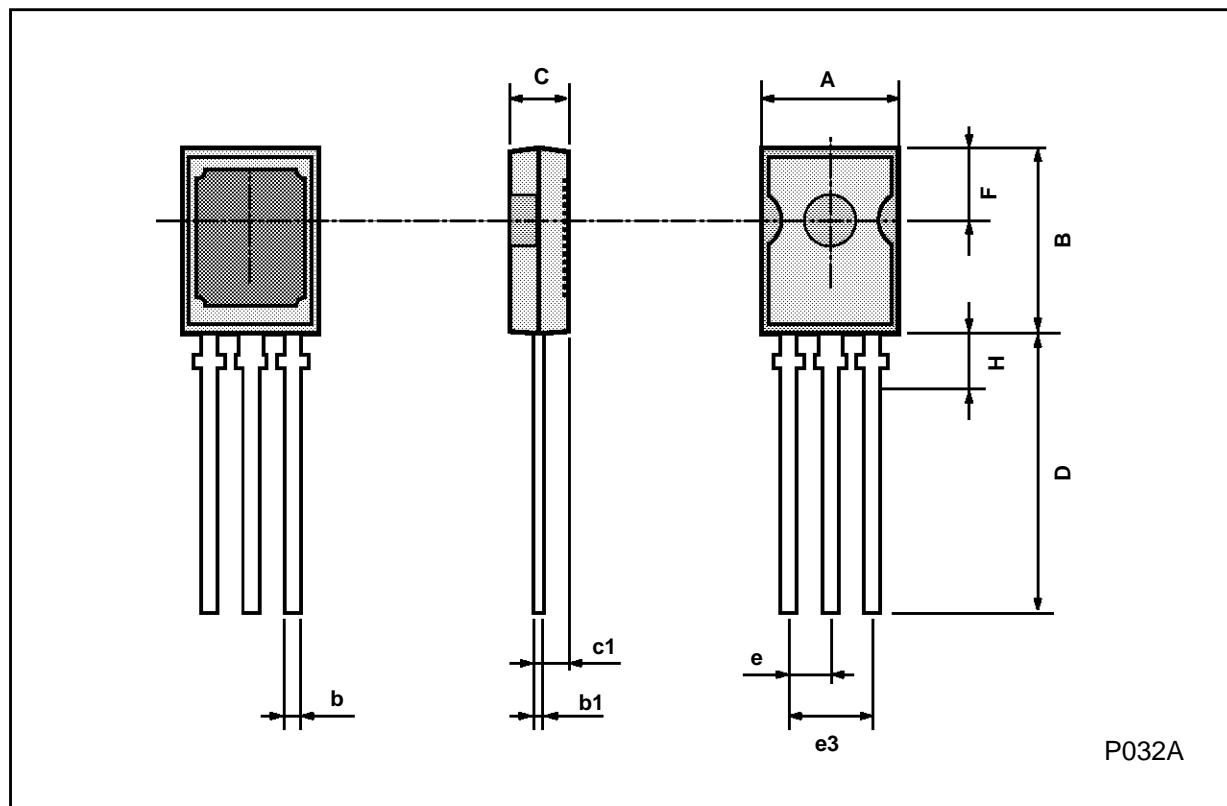


Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time



SOT-82 MECHANICAL DATA

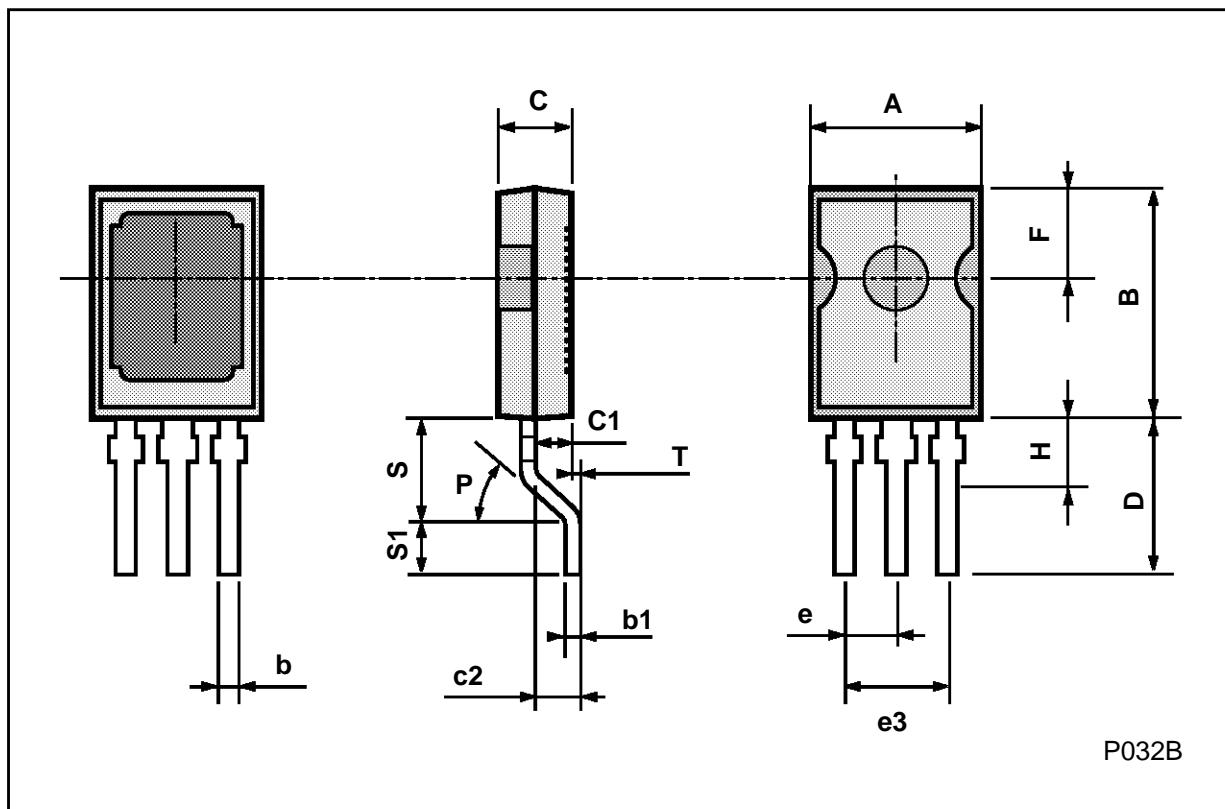
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		11.3	0.413		0.445
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.04		0.106
c1		1.2			0.047	
D		15.7			0.618	
e		2.2			0.087	
e3		4.4			0.173	
F		3.8			0.150	
H			2.54		0.100	



P032A

SOT-194 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		11.3	0.413		0.445
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.094		0.106
c1		1.2			0.047	
c2		1.3			0.051	
D		6			0.236	
e		2.2			0.087	
e3		4.4			0.173	
F		3.8			0.150	
H			2.54			0.100
P	45° (typ.)					
S		4			0.157	
S1		2			0.079	
T		0.1			0.004	



P032B

STK12N05L/STK12N06L

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